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10/639,350	08/12/2003	Robert M. Crosby	TI-34618	6171

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/639,350	CROSBY, ROBERT M.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *5,6 and 11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-10 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *03/01/07*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

Group I.

Claims 1-4, drawn to:

a) A memory unit comprising a memory portion having storage units storing data bits; a memory portion storing error correction bits; an error checking and correction unit; and registers to hold the location of one or more corrected bits are classified in 714/758.

Claims 7-10, drawn to:

b) A data processing system, the data processing system comprising a central processing unit; and a memory unit, the memory unit including a main memory, the main memory storing data signal groups in a plurality of addresses; an error checking and correction memory, the error checking and correction memory storing error correcting signals for each data signal group in the main memory at the same address in the error checking and correction code memory; error checking and correction apparatus for identifying and correcting at least one error in a data group accessed by a read operation; and failing bit apparatus, the failing bit apparatus identifying when a correctable error is the result of a failing location are classified in 714/758.

Claims 14-17, drawn to:

c) A memory unit comprising a non-volatile main memory unit; a non-volatile error memory for storing error checking and correction signals for a signal group in the main memory having the same address; error checking and correction apparatus, the error apparatus generating a correction pattern identifying the location of an error in an addressed signal group and the associated error signals, the error apparatus generating a restore signal when the error is consistent with a failing bit location; flag apparatus storing the associated correction pattern and the associated address in response to the restore signal, the flag apparatus generating an interrupt flag in response to the restore signal are classified in 714/758 .

Group II.

Claims 5 and 6, drawn to:

A memory unit comprising storage units storing data bits; storage units storing error checking and correction bits; and an error detection and correction unit wherein the memory unit contains circuitry to optionally exclude the condition where all of the data bits and error detection and correction bits are in the erased state from generating bit correction (as in claim 5) and a memory unit comprising storage units for storing data bits; storage units for storing error correction bits; an error detection and correction unit; circuitry to optionally exclude the condition where all of the

data bits and error detection and correction bits are in the programmed state from generating bit correction (as in claim 6) classified in 714/763.

Group III.

Claims 11-13, drawn to:

A method of responding to an error in a signal group retrieved from a non-volatile memory unit, the method comprising when the error is correctable, correcting the error in the signal group using error checking and correction techniques; and when the error is consistent with a failing bit position, restoring the charge associated with the bit position classified in 714/764.

The invention are distinct, each from the other because of the following reasons: Invention Group I, Group II and Group III are related as subcombinations disclosed **as usable together in a single combination.** The subcombinations are distinct from each other if they are shown to be separately usable.

In the instance case, invention Group I has separate utility separate utility for storing and holding (in a register) error correction and detection bits in a memory unit and further identifying and correcting at least one error in a data group accessed by a read operation; and failing bit apparatus, the failing bit apparatus identifying when a correctable error is the result of a failing location and furthermore an error apparatus generating a restore signal when the error is consistent with a failing bit location; flag apparatus storing the associated correction pattern and the associated address in response to the restore signal, the flag apparatus generating an interrupt flag in response to the restore signal.

In the instant case, the invention of Group II has separate utility such as storing error checking and correction bits; and an error detection and correction unit wherein the memory unit contains circuitry to optionally exclude the condition where all of the data bits and error detection and correction bits are in the erased or in the programmed state from generating bit correction.

In the instant case, the invention of Group III has separate utility separate utility for such as a method of responding to an error in a signal group retrieved from a non-volatile memory unit, the method comprising when the error is correctable, correcting the error in the signal group using error checking and correction techniques; and when the error is consistent with a failing bit position, restoring the charge associated with the bit position.

Because these inventions are distinct for the reason given above and the search required for Group I is not required for Group II and Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group II is not for Group I and Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group III is not for Group I and Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. William W. Holloway on 01 March of 2007 a provisional election was made with out traverse to prosecute the invention of Group I, claims 1-4, 7-10 and 14-17.

Affirmation of the election must be made by applicant in replying to this office action. Claims 5, 6 and 11-13 are withdrawn from further consideration by the examiner 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the specification. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

1. Claims **1-4, 7-10 and 14-17** are presented for examination.

Priority

2. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 119(e), through provisional applications 60/470,783 filed 05/15/03.

Oath Declaration

3. The oath/declaration filed on 08/12/03 is acceptable.

Drawings

4. The drawings are objected to because:

a) figure 1 should be designated by a legend such as – **prior art** - in order to clarify what is applicant's invention (see MPEP 608.02(g).

b) The **informal drawings** filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

A proposed drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Corrected drawings sheets in compliance with 37 CFR 1.121(d) are required in reply to the office action should include all the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended". If a drawing figure is to be cancelled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheet may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header so as not to obstruct any portion of the drawing figures. If the changes are not acceptable by the examiner, the applicant will be notified and informed of any required corrective action in the next office action. The objection to the drawings will not be held in abeyance.

Claim objections

5. Claim 1 is objected to because of the following informalities:

- In lines 2 and 3, there needs to be "for" prior to "storing data bits" and "for" prior to "storing error correction".

Claim 7 is objected to because of the following informalities:

- In lines 24 and 27, there needs to be "an" prior to "error checking and correction" and "a" prior to "failing bit apparatus".

Claim 14 is objected to because of the following informalities:

- In lines 12 and 16, there needs to be "an" prior to "error checking and correction" and "a" prior to "a flag apparatus".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims **2, 4 and 8** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites, the phrase **"can be polled " and "can be corrected"** are indefinite (see line 3).

Claim 4 recites; the phrase **"can be set" is** indefinite (see line 2).

Claim 4 recites; the phrase **"may be changed" is** indefinite (see line 3).

Claim 8 recites, the phrase **"can be the result" is** indefinite (see line 6).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims **1-4, 7-10 and 14-17** are rejected under 35 U.S.C. **102(b)** as being clearly anticipated by Abdoo et al. (hereafter referred to as Abdoo) (U.S. PN: 5,490,155).

As per claim 1:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR

signal and the NCERR signal) which controls the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67) and when either the CERR signal or the NCERR signal is asserted, the syndrome bits are stored in a diagnostic resister in the SDB (44, 45) that generated them. The register includes a series of other diagnostic bits, including a bit, which indicates whether the error occurred during a read cycle or a read-merge-write cycle (registers to hold the location of one or more bits).

As per claims 2-4:

Abdoo substantially teaches or discloses that when an error occurs, the computer system stores various data regarding the error so that the cause of the error may be analyzed. Both the CERR signal and the NCERR signal are provided to the CSP (46), which controls the interrupts to the various CPUs in the computer system. If the CERR signal is asserted, the CSP (46) asserts an interrupt request (IRQ) signal, indicating that a correctable error has occurred (see col. 11, lines 62-67).

As per claims 7 and 8:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses that the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection

correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a failing bit apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR signal and the NCERR signal) which controls the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67).

As per claim 9:

Abdoo teaches a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11).

As per claim 10:

Abdoo in figure 1 teaches that the computer system comprising an EISA bus 42 is coupled through buffers 56 to a bus referred to as the X bus 60. A number of peripheral devices are coupled to the X bus 60, including a keyboard controller 62, a real time clock (RTC) 64, and an electrically erasable programmable read only memory (EEPROM) 66, (see col. 4, lines 44-54).

As per claims 14:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors

are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a flag apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR signal and the NCERR signal) which controls the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67).

As per claims 15 and 16:

Abdoo further in figure 1 discloses that the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a flag apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these

interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22).

As per claim 17:

Abdoo in figure 1 discloses that the computer system comprising an EISA bus 42 is coupled through buffers 56 to a bus referred to as the X bus 60. A number of peripheral devices are coupled to the X bus 60, including a keyboard controller 62, a real time clock (RTC) 64, and an electrically erasable programmable read only memory (EEPROM) 66, (see col. 4, lines 44-54).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,272,651 Chin et al.

US PN : 6,505,305 Olarig, Sompong

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status

information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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